ORIENT

Photo coupler

Product Data Sheet

Part Number: OR-341(B)

Customer: _____

Date: _____

一级代理商：

深圳市弗瑞鑫电子有限公司

地址：深圳市宝安区西乡大道302号金源商务大厦B座三楼

0 -

0 - 0 0

.frxelec.

opyright© 2020 Orient .All rights Reserved

1.

(1) 3.0 A maximum peak output current
(2) 2.5 A minimum peak output current
(3) Rail-to-rail output voltage
(4) 200 ns maximum propagation delay
(5) 70 ns maximum propagation delay difference
(6) LED current input with hysteresis
(7) 20 kV/μs minimum Common Mode Rejection (CMR) at VCM = 1500 V
(8) I_{CC} = 3.0 mA maximum supply current
(9) Under Voltage Lock-Out protection (UVLO) with hysteresis
(10) Wide operating V_{CC} Range: 15 to 30 V
(11) Industrial temperature range: -40° C to 105° C
(12) Safety approval
UL approved(No.E323844)
VDE approved(No.40029733)
CQC approved (No.CQC19001231480)
(13) In compliance with RoHS, REACH standards
(14) MSL Level 1

2.

The OR-341(B) contains an AlGaAs LED, which is optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate controlled devices. The voltage and high peak output current supplied by this optocoupler make it ideally suited for direct driving IGBT with ratings up to 1200 V/ 100 A. For IGBTs with higher ratings, this optocoupler can be used to drive a discrete power stage which drives the IGBT gate.

3.

(1)IGBT/MOSFET gate drive (2)AC and Brushless DC motor drives
(3)Renewable energy inverters (4)Industrial inverters (5)Switching power supplies

4.

LED	VCC – VEE “POSITIVE GOING” (i.e., TURN-ON)	VCC – VEE “NEGATIVE GOING” (i.e., TURN-OFF)	VO
OFF	0		

Note: A 1 F bypass capacitor must be connected between pins V_{CC} and V_{EE}.

opyright© 2020 Orient .All rights Reserved

5.

Input	Average Forward Input Current	I_F	25	mA
	Reverse Input Voltage	V_R	5	V
Output	“High” Peak Output Current	$I_{OH(PEAK)}$	3	A
	“Low” Peak Output Current	$I_{OL(PEAK)}$	3	A
	Output Collector Power Dissipation	P_O	700	mW
Total Power Dissipation		P_T	745	mW
Total Output Supply Voltage		V_{CC} - V_{EE}	35	V
Input Current (Rise/Fall Time)		$t_{r(IN)}$ / $t_{f(IN)}$	500	ns
Insulation Voltage		Viso	5000	Vrms
Working Temperature		T_{opr}	-40 + 105	
Storage Temperature		T_{stg}	-55 + 125	
*2 Soldering Temperature		T_{sol}	260	

*1. Room temperature = 25 . Exceeding the maximum absolute rating can permanently damage the device. Working long hours at the maximum absolute rating can affect reliability.

*2. soldering time is 10 seconds.

opyright© 2020 Orient .All rights Reserved

6.

Unless otherwise noted, all typical values are at TA = 25° C, VCC - VEE = 30 V, VEE = Ground; all minimum and maximum specifi cations are at recommended operating conditions (TA = -40 to 105° C, IF(ON) = 7 to 16 mA, VF(OFF) = -3.6 to 0.8 V, VEE = Ground, VCC = 15 to 30 V).

High Level Output Current	I_{OH}	-1.0	-2.3	—	A	$V_O = (V_{CC} – 4V)$
		-2.5	—	—		$V_{CC}– V_O ≤15V$
Low Level Output Current	I_{OL}	1.0	2.5	—	A	$V_O = (V_{EE} + 2.5V)$
		2.5	—	—		$V_{CC}– V_O ≤15V$
High Output Transistor RDS(ON)	$R_{DS,OH}$	—	1.7	3.0		I_{OH} = -2.5 A
Low Output Transistor RDS(ON)	$R_{DS,OL}$	—	0.8	1.8		I_{OH} = 2.5 A
High Level Output Voltage	V_{OH}	(V_{CC} – 0.3)	(V_{CC} – 0.2)	—	V	I_O = –100 mA
		—	V_{CC}	—	V	I_O = 0 mA, I_F = 10 mA
Low Level Output Voltage	V_{OL}	—	0.06	0.2	V	I_O = 100 mA
High Level Supply Current	I_{CCH}	—	1.51	3.0	mA	R_g=10 ,C_g = 25 nF, I_F=10 mA
Low Level Supply Current	I_{CCL}	—	1.65	3.0	mA	R_g =10 ,C_g=25nF, V_F=0 V
Threshold Input Current Low to High	I_{FLH}	—	1.89	4.0	mA	R_g=10 ,C_g=25nF, V_O>5 V
Threshold Input Voltage High to Low	V_{FHL}	0.8	—	—	V	
Input Forward Voltage	V_F	1.2	1.55	1.95	V	I_F = 10 mA
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$	—	–1.7	—	mV/°C	I_F = 10 mA
Input Reverse Breakdown Voltage	B_{VR}	5	—	—	V	I_R = 100 µA
Input Capacitance	C_{IN}	—	70	—	pF	f = 1 MHz, V_F = 0V
UVLO Threshold	V_{UVLO+}	11.0	12.7	13.5	V	V_O > 5 V I_F = 10 mA
	V_{UVLO-}	9.5	11.2	12.0		
UVLO Hysteresis	$U_{VLO_{HYS}}$	—	1.5	—		

opyright© 2020 Orient .All rights Reserved

7.

Unless otherwise noted, all typical values are at TA = 25° C, VCC - VEE = 30 V, VEE = Ground; all minimum and maximum specifi cations are at recommended operating conditions (TA = -40 to 105° C, IF(ON) = 7 to 16 mA, VF(OFF) = -3.6 to 0.8 V, VEE = Ground, VCC = 15 to 30 V).

Propagation Delay Time to High Output Level	t_{PLH}	50	140	200	ns	R_g = 10 C_g = 25 nF f = 20 kHz Duty Cycle = 50% I_F = 7 mA to 16 mA V_{CC} = 15 V to 30 V
Propagation Delay Time to Low Output Level	t_{PHL}	50	140	200	ns	
Pulse Width Distortion	PWD	—	25	70	ns	
Propagation Delay Difference Between Any Two Parts	P_{DD} ($t_{PHL} - t_{PLH}$)	–100	—	100	ns	
Rise Time	t_r	—	46	—	ns	V_{CC} = 30 V
Fall Time	t_f	—	43	—	ns	
Output High Level Common Mode Transient Immunity	$\|CM_H\|$	20	30	—	kV/µs	T_A= 25°C, I_F =10mA V_{CC}=30V, V_{CM} =1500V with split resistors
Output Low Level Common Mode Transient Immunity	$\|CM_L\|$	20	30	—		T_A=25°C, V_F=0V, V_{CC}=30V, V_{CM}=1500V with split resistors

8.

341= Part Number

(B)= Identification.

U = Lead form option, W or W1

Y = Tape and reel option (TA,TA1 or none).

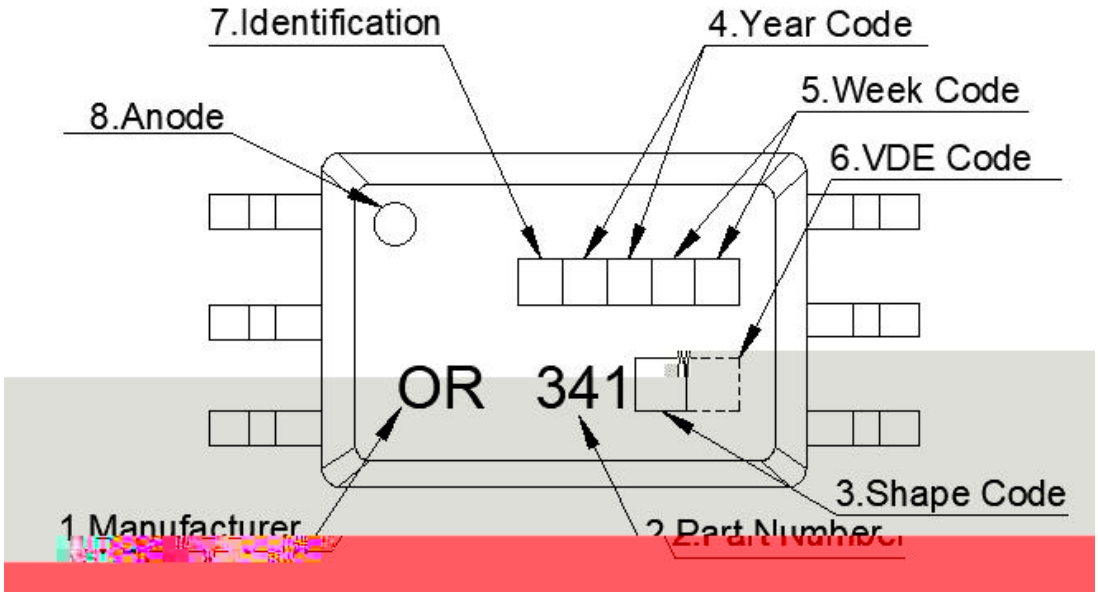
Z = ‘V’ code for VDE safety (This options is not necessary).

* VDE Code can be selected.

S(TA)	Surface mount lead form (low profile) + TA tape & reel option	1000 units per reel
S(TA1)	Surface mount lead form (low profile) + TA1 tape & reel option	1000 units per reel

opyright© 2020 Orient .All rights Reserved

9.



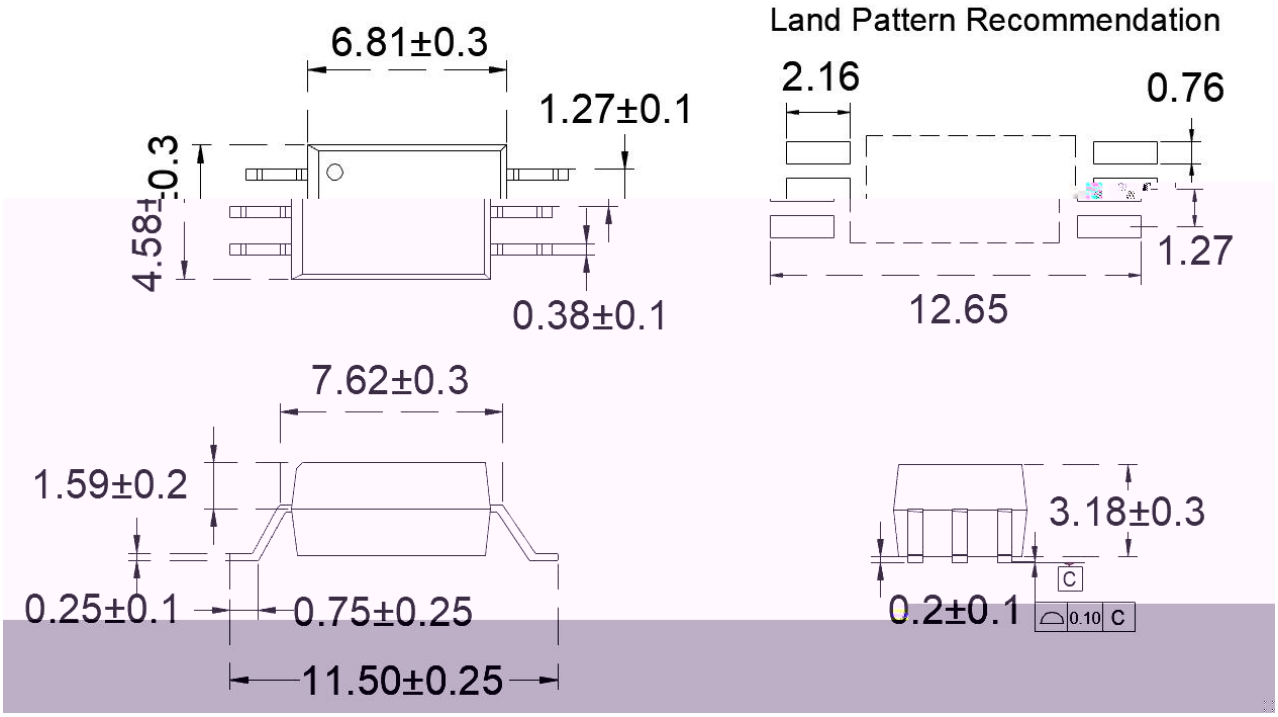
1. Manufacturer : ORIENT.
2. Part Number : 341.
3. Shape Code ☐ : Lead form option ,W or W1 .
4. Year Code ☐☐ '21' means '2021' and so on.
5. Week Code ☐☐ 01 means the first week, 02 means the second week and so on.
6. VDE Code ☐. (Optional)
7. Identification.
8. Anode.

* VDE Mark can be selected.

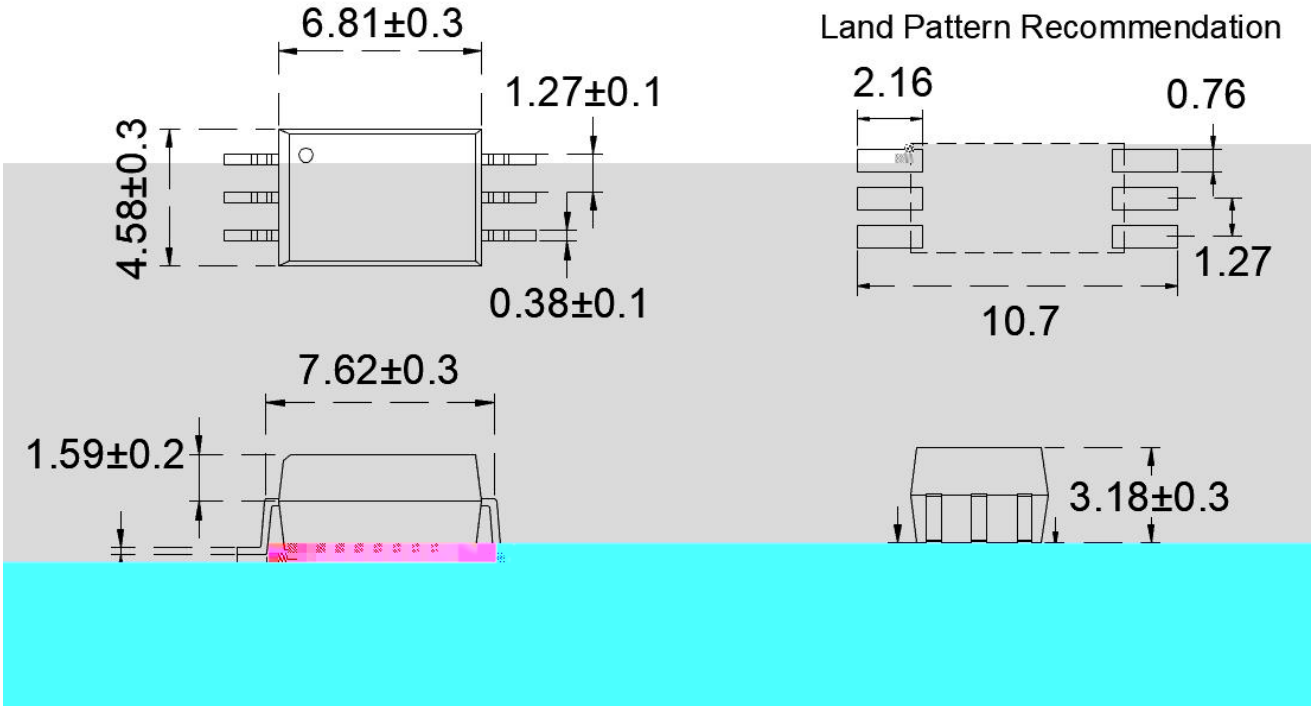
opyright© 2020 Orient .All rights Reserved

10.

(1).OR-341(B)W



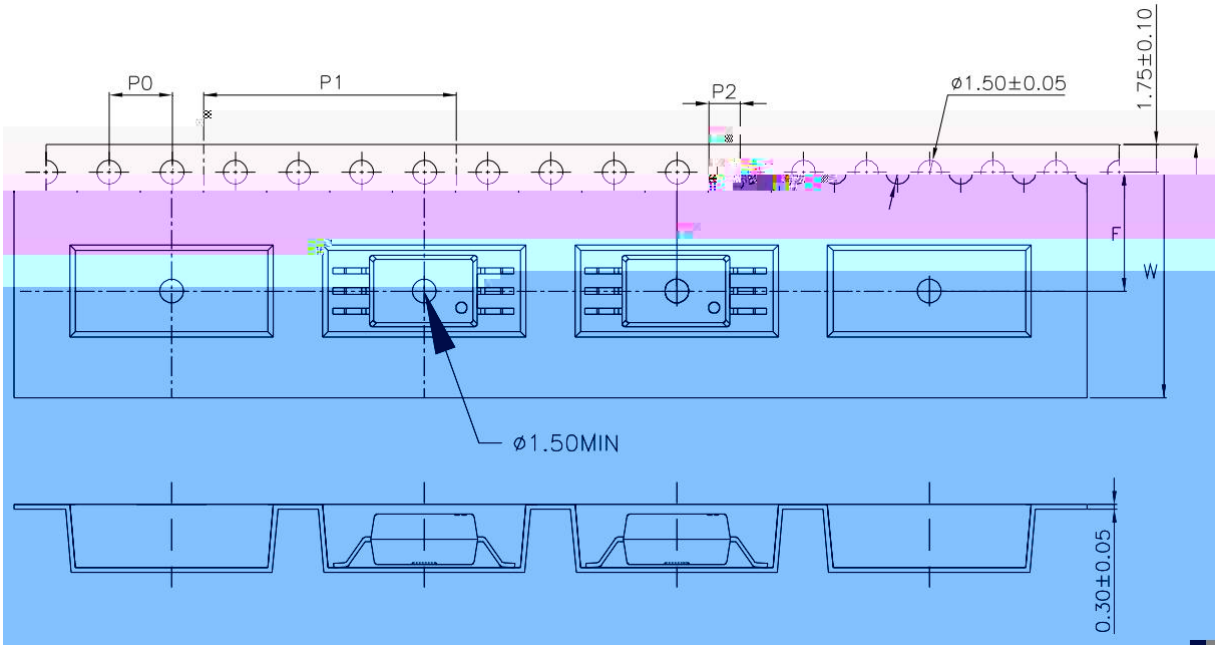
(2).OR-341(B)W1



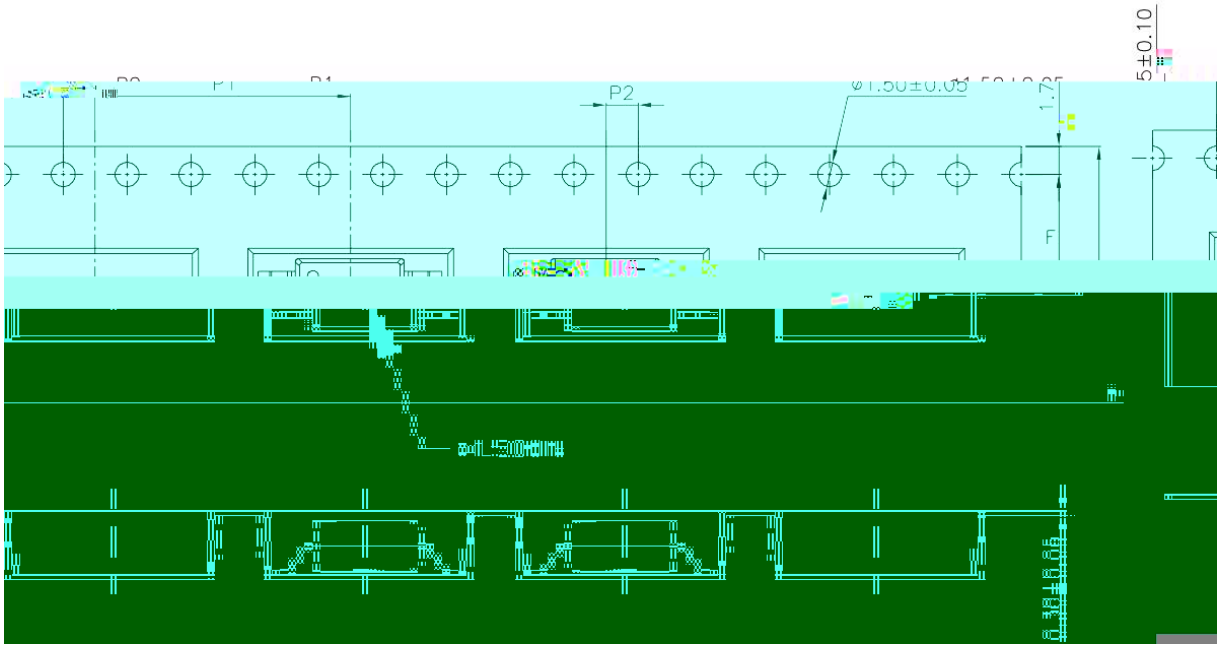
opyright© 2020 Orient .All rights Reserved

11.

(1)OR-341(B)W-TA

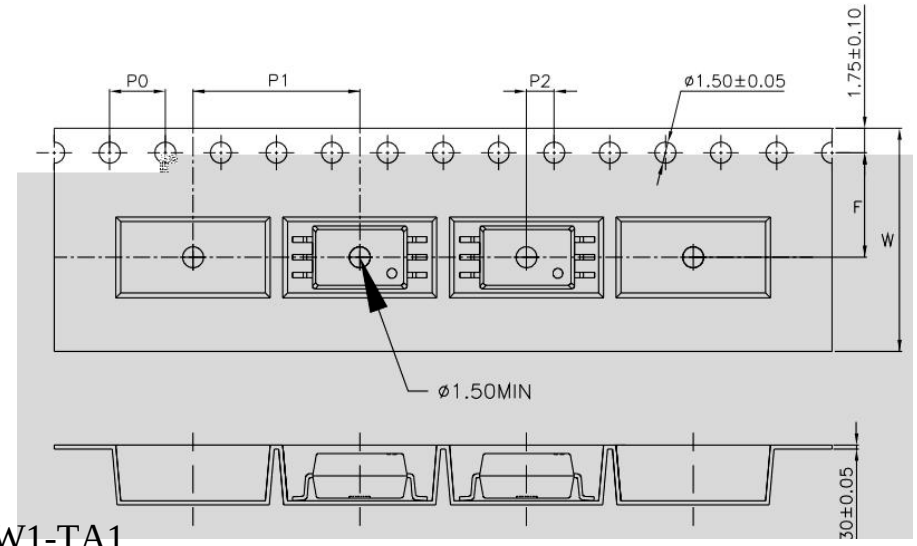


(2)OR-341(B)W-TA1

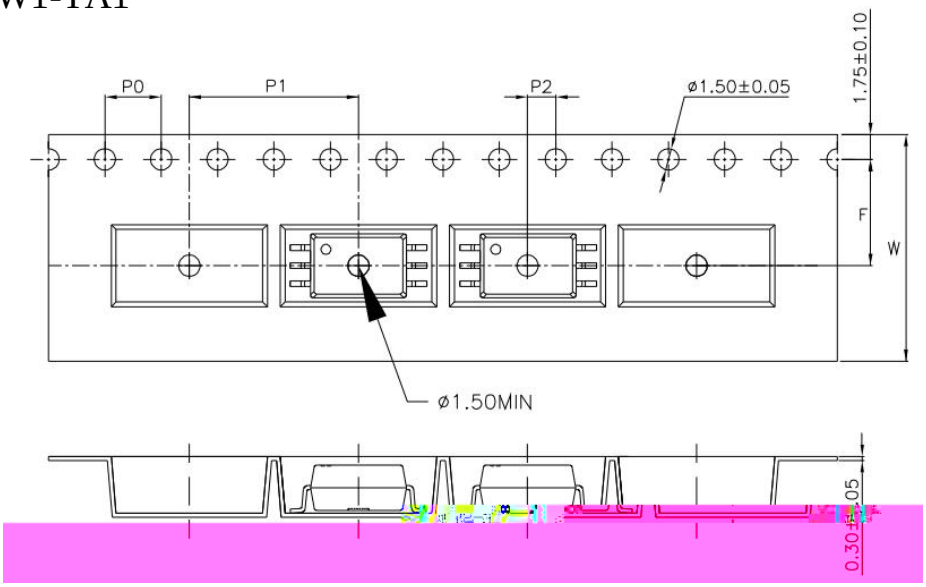


opyright© 2020 Orient .All rights Reserved

(1)OR-341(B)W1-TA



(2)OR-341(B)W1-TA1



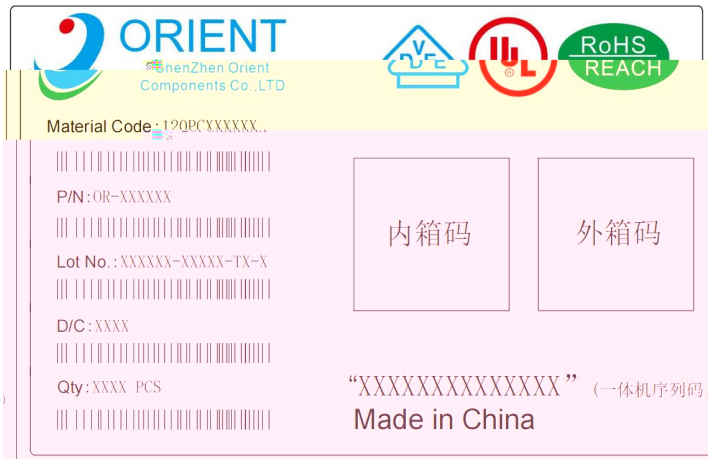
Type	symbol		
bandwidth	W	16±0.3 (0.63)	16±0.3 (0.63)
pitch	P0	4±0.1 (0.16)	4±0.1 (0.16)
pitch	F	7.5±0.1 (0.3)	7.5±0.1 (0.3)
	P2	2±0.1 (0.079)	2±0.1 (0.079)
interval	P1	16±0.1 (0.63)	12±0.1 (0.47)

Encapsulation type	TA/TA1
amount pcs	1000

opyright© 2020 Orient .All rights Reserved

12.

Packing type	Reel type
Tape Width	16mm
Qty per Reel	1,000pcs
Small box (inner) Dimension	345*345*58.5mm
Large box (Outer) Dimension	620x360x360mm
Max qty per small box	2,000pcs
Max qty per large box	20,000pcs



1. Material Code :Product ID.
2. P/N :Contents with "Order Information" in the specification.
3. Lot No. :Product data.
4. D/C :Product weeks.
5. Quantity :Packaging quantity.

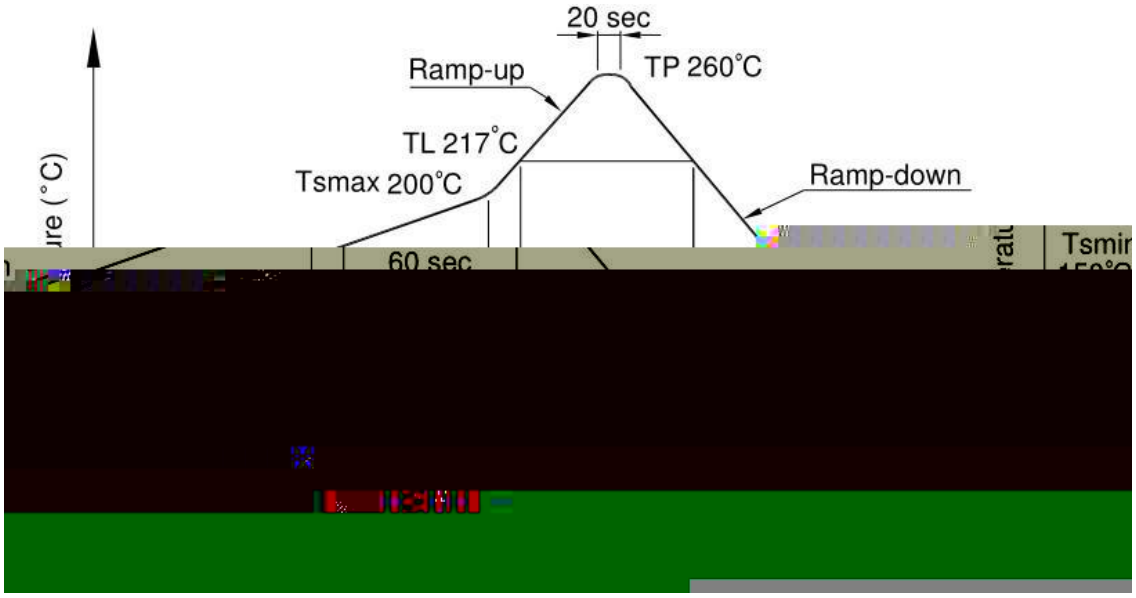
opyright© 2020 Orient .All rights Reserved

13.

(1).IR Reflow soldering (JEDEC-STD-020C compliant)

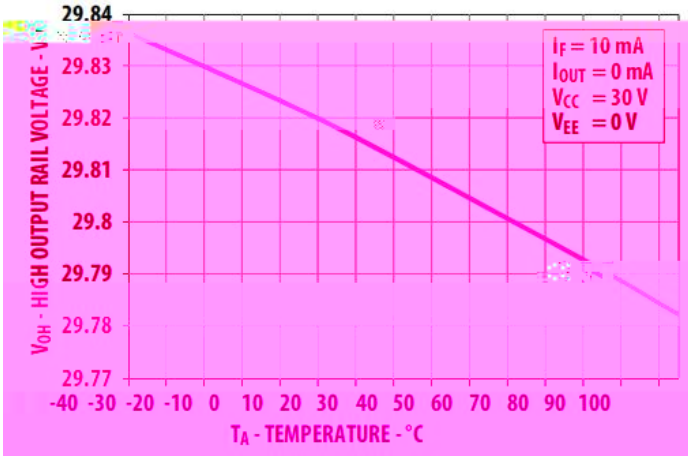
One time soldering reflow is recommended within the condition of temperature and time profile shown below. Do not solder more than three times.

Preheat - Temperature Min (T Smin) - Temperature Max (T Smax) - Time (min to max) (ts)	 150˚C 200˚C 90±30 sec
Soldering zone - Temperature (TL) - Time (t L)	 217˚C 60 sec
Peak Temperature	260˚C
Peak Temperature time	20 sec
Ramp-up rate	3˚C / sec max.
Ramp-down rate from peak temperature	3~6˚C / sec
Reflow times	≤3



opyright© 2020 Orient .All rights Reserved

14.



re 1. High output rail voltage vs. temperature

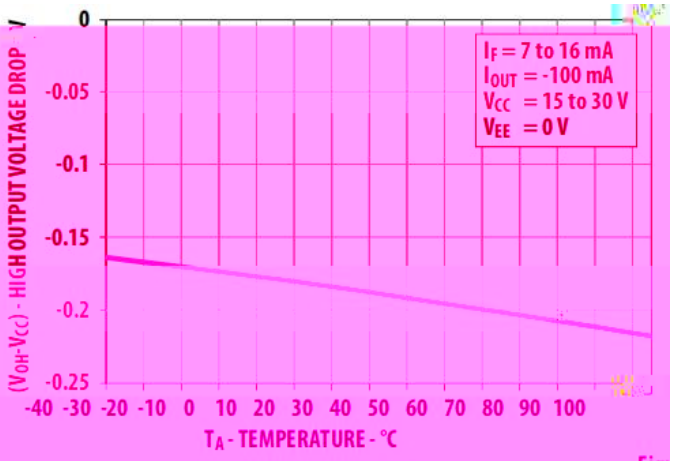
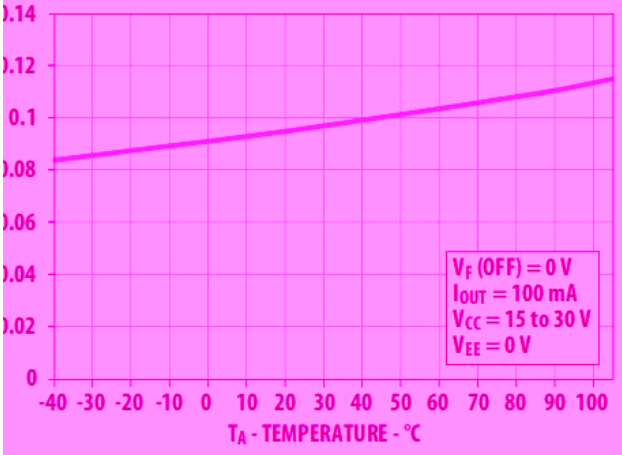


Figure 2. V_{OH} vs. temperature



re 3. V_{OL} vs. temperature

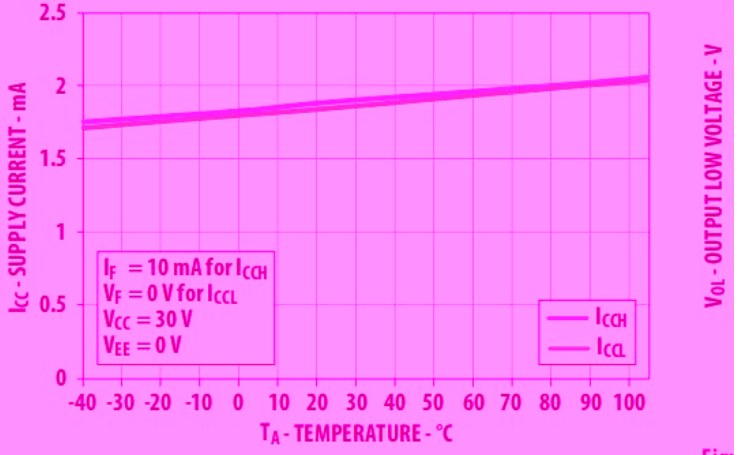
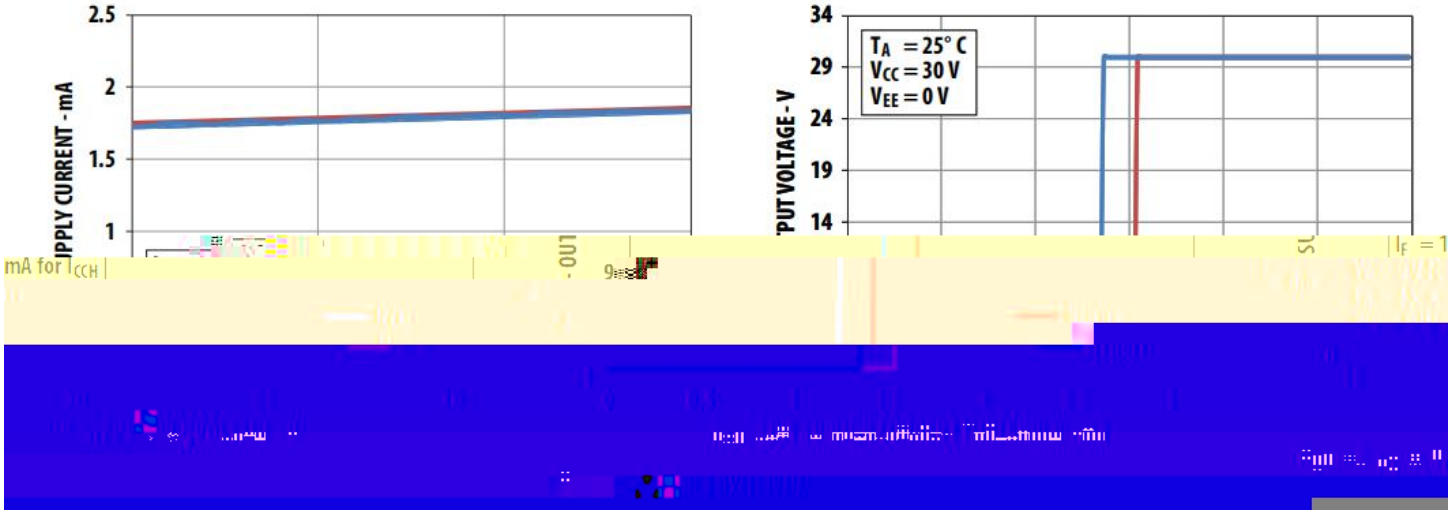


Figure 4. I_{CC} vs. temperature



opyright© 2020 Orient .All rights Reserved

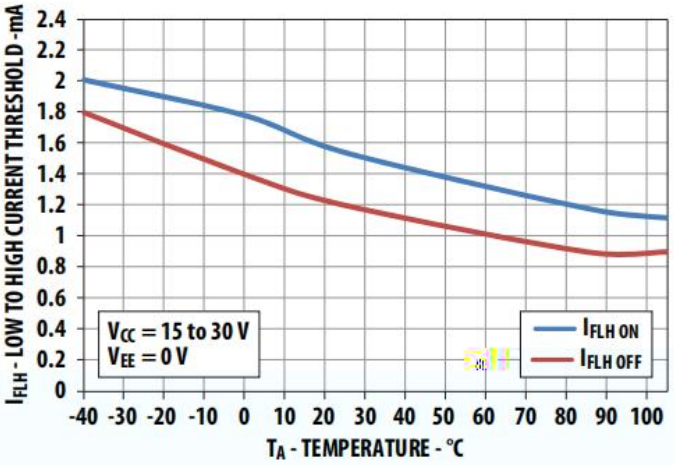


Figure 7. I_{FLH} vs. temperature

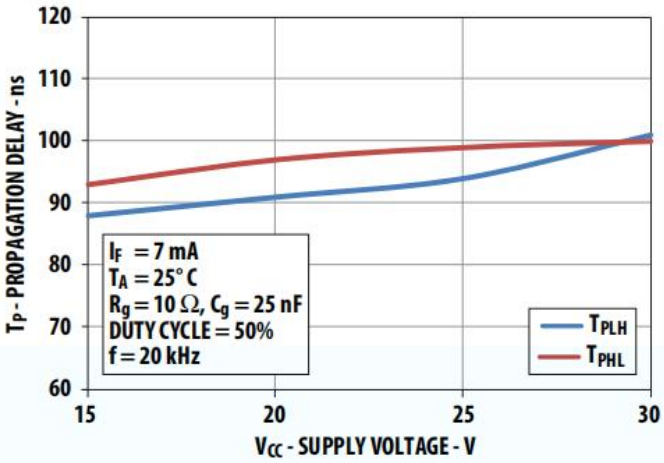


Figure 8. Propagation delays vs. V_{CC}

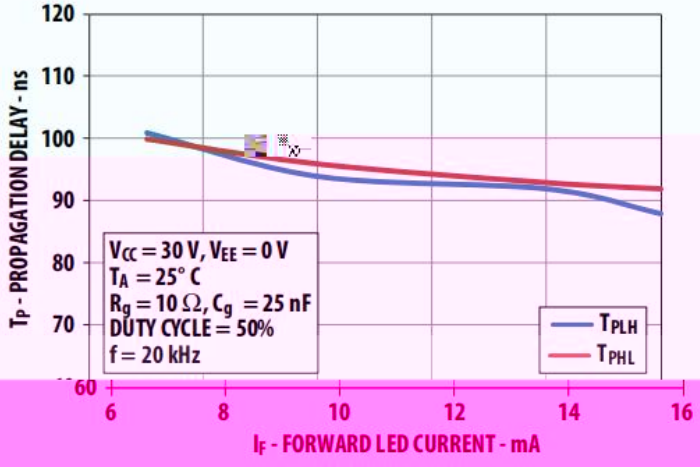


Figure 9. Propagation delays vs. I_F

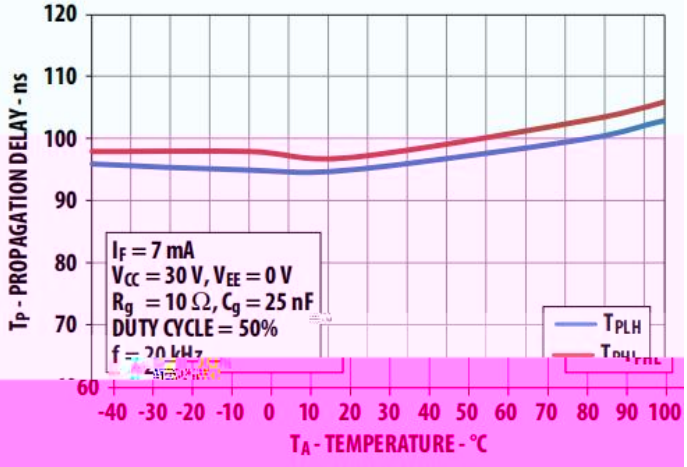


Figure 10. Propagation delays vs. temperature

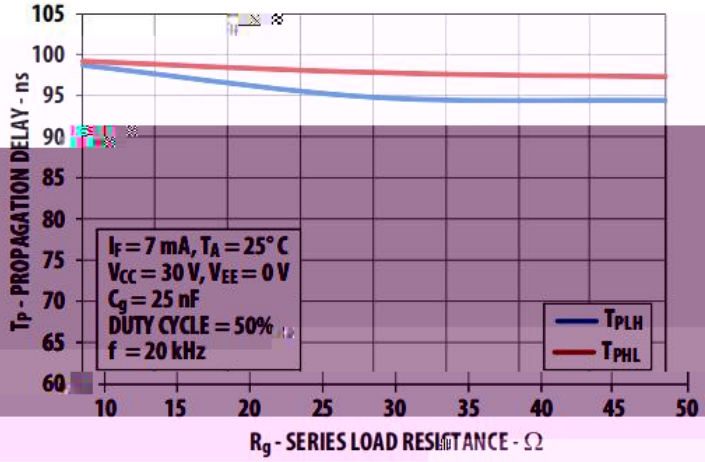


Figure 11. Propagation delay vs. Rg

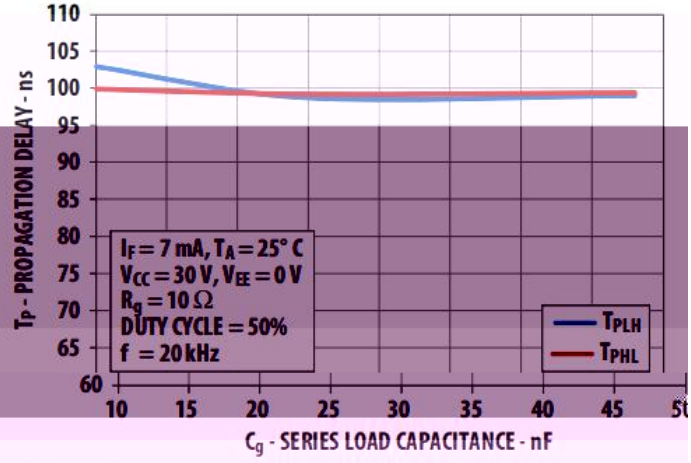


Figure 12. Propagation delay vs. Cg

opyright© 2020 Orient .All rights Reserved

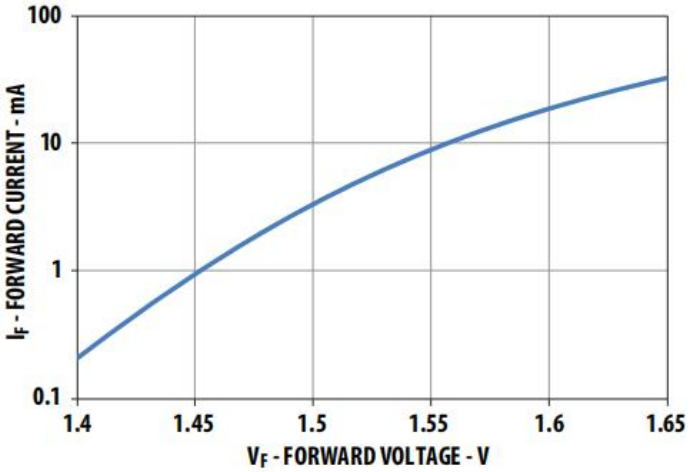
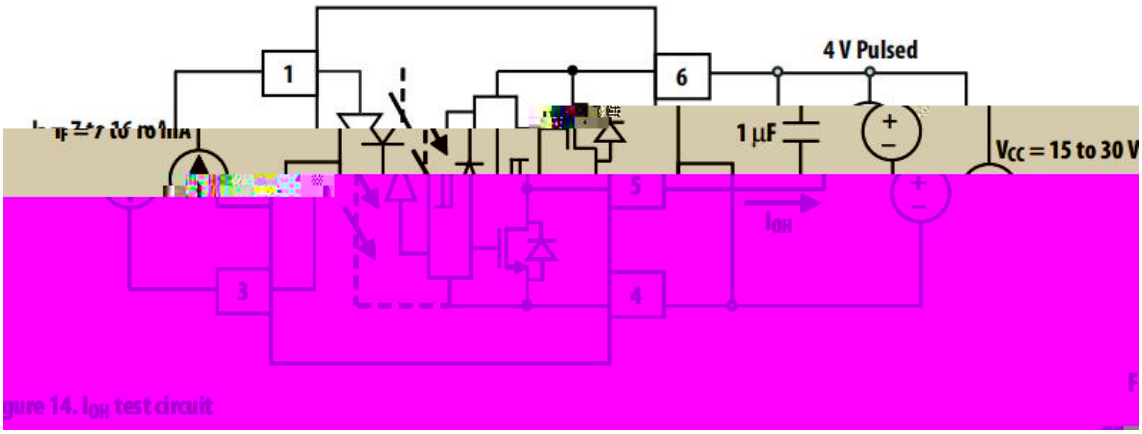


Figure 13. Input current vs. forward voltage



gure 14. I_{OH} test circuit

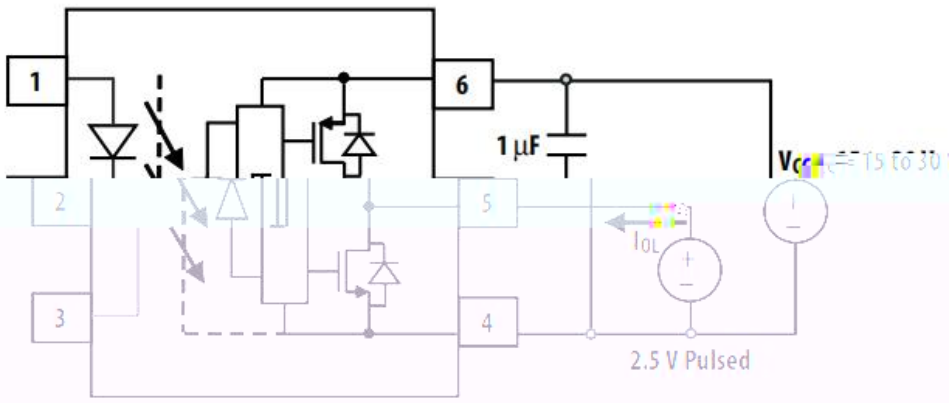


Figure 15. I_{OL} test circuit

opyright© 2020 Orient .All rights Reserved

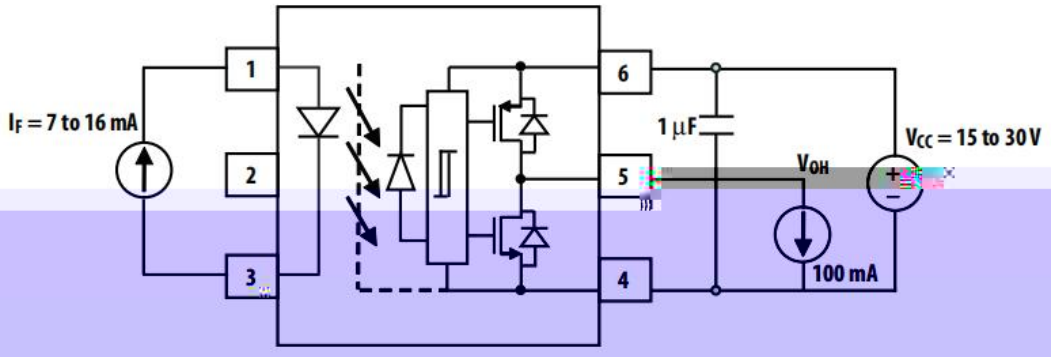


Figure 16. V_{OH} test circuit

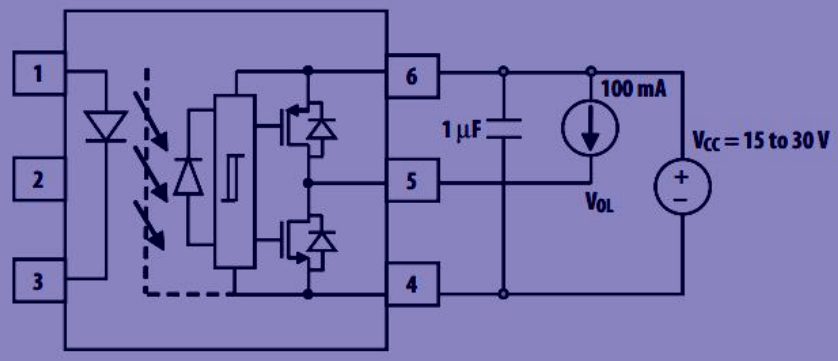


Figure 17. V_{OL} test circuit

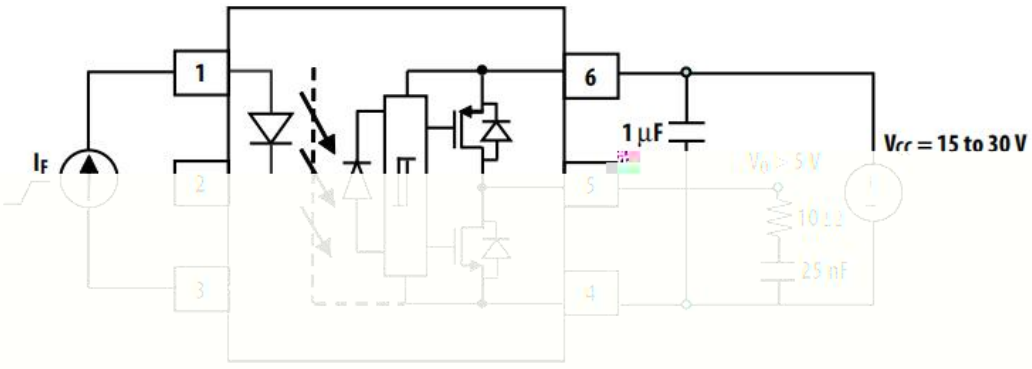


Figure 18. I_{FLH} test circuit

opyright© 2020 Orient .All rights Reserved

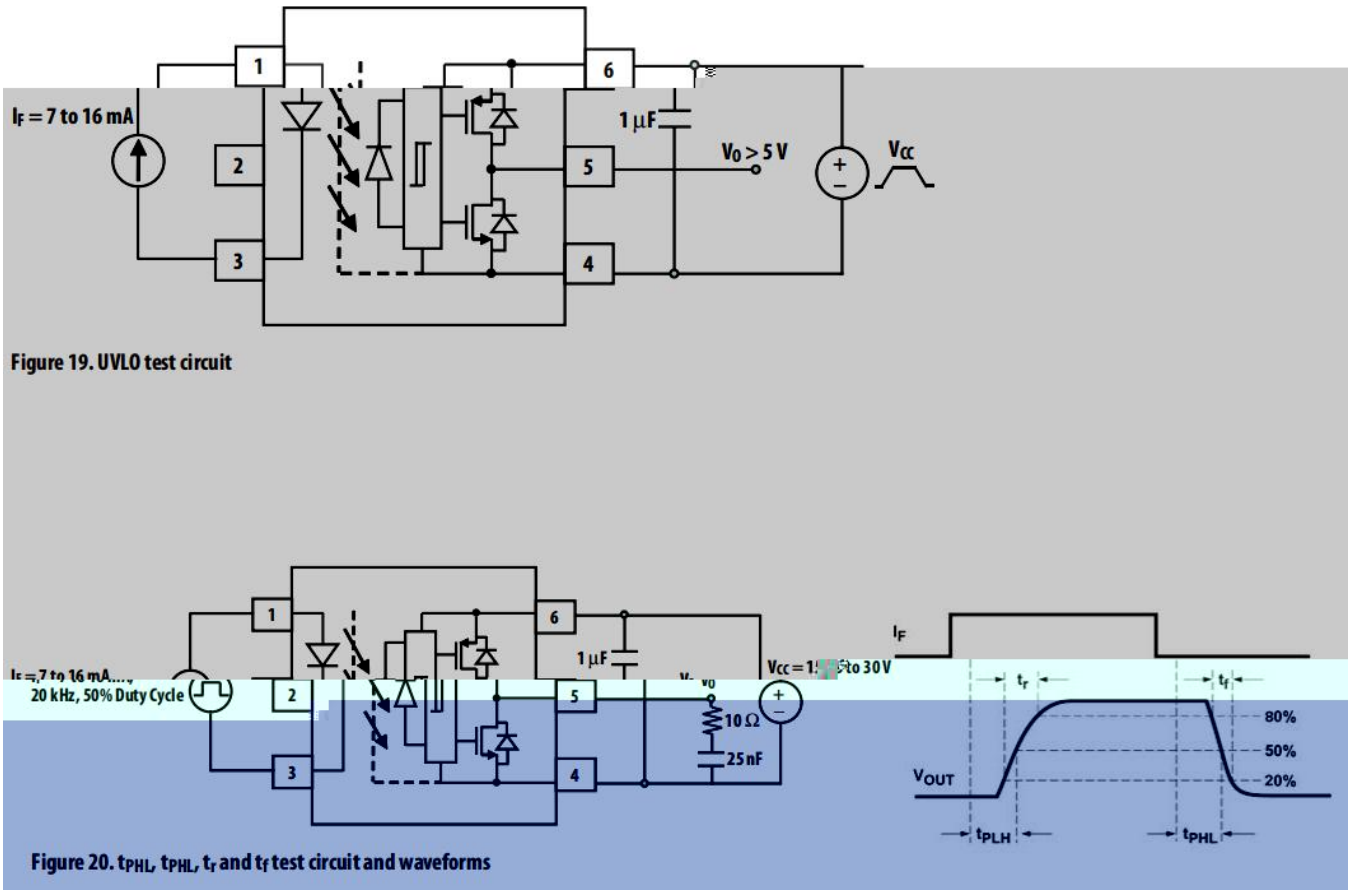


Figure 19. UVLO test circuit

Figure 20. t_{PHL}, t_{PHL}, t_r and t_f test circuit and waveforms

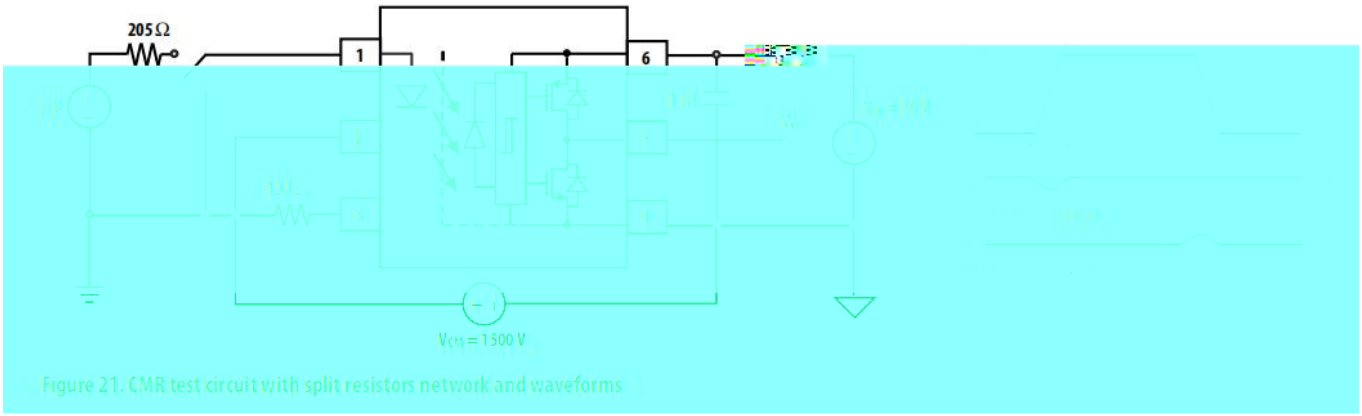


Figure 21. CMR test circuit with split resistors network and waveforms

opyright© 2020 Orient .All rights Reserved